Lithium-Ion Battery Monitor

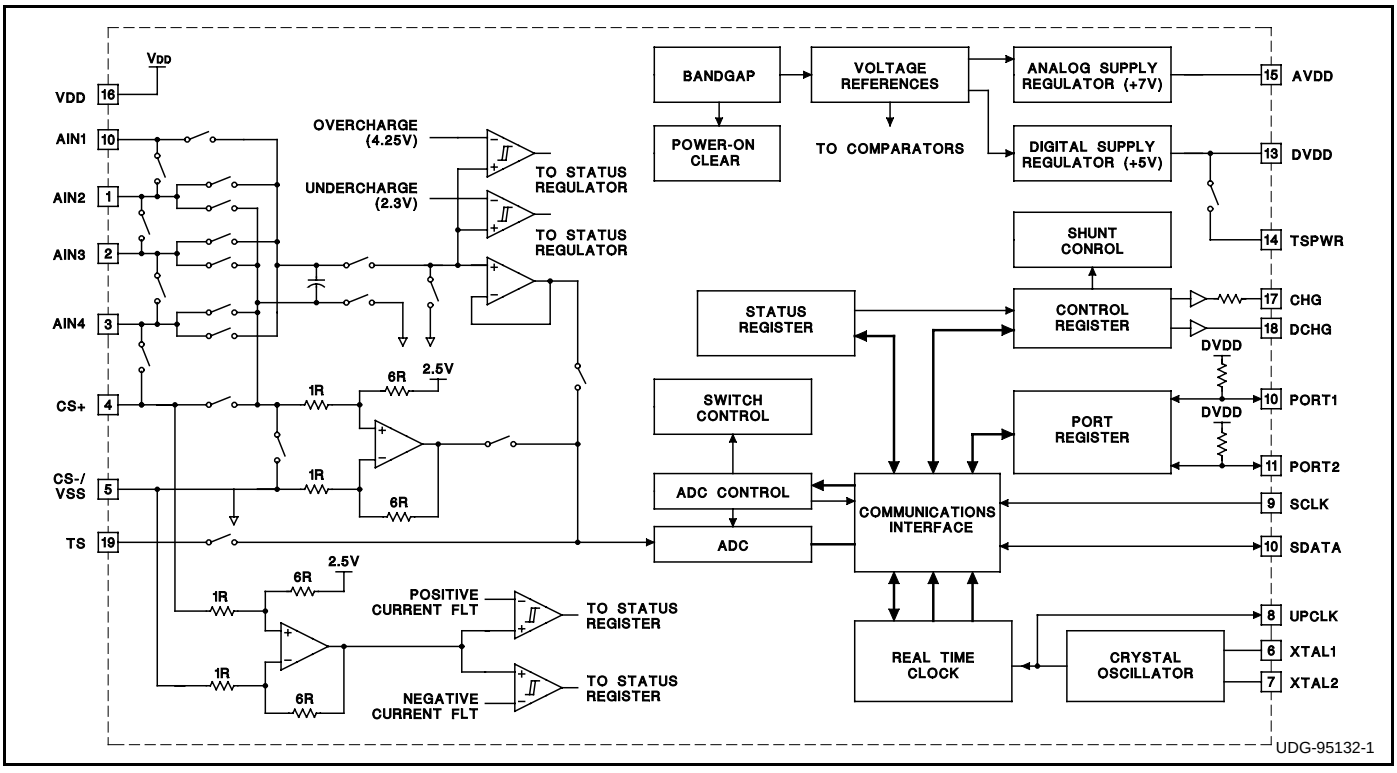
FEATURES

- Measures Individual Cell Voltage for Three or Four Lithium-Ion Cells
- Measures Battery Pack Current and Temperature
- 10 Bit A/D with Microprocessor Interface
- Hardware Overcharge, Over-Discharge, and Overcurrent Protection
- Communications Interface for Optional External EEPROM
- Two Year Real Time Clock
- Regulated 5V Microprocessor Supply

DESCRIPTION

The UCC3951 is a monolithic BCDMOS integrated circuit designed to reside inside a battery pack and measure under host microprocessor control any combination of battery parameters, such as cell voltage, pack current, and pack temperature. The UCC3951 is designed for the unique charging and safety concerns associated with lithium-ion cells, and includes protection features such as programmable current shunts for individual cell charge equalization, hardware monitoring of individual cell voltage and pack current, and isolation of the cells from charge and/or discharge currents.The UCC3951 is intended to be paired with a simple, low-cost host microprocessor such as an 80C51, that resides either inside or outside the battery pack. If the microprocessor is external to the pack, an optional serial EEPROM can be used inside the pack to retain battery information, such as number of cycles, pack serial numbers, or system calibration constants. The UCC3951 provides the clock to the host microprocessor and a regulated power source to the host, EEPROM and the thermistor. Operation of the 32kHz crystal during sleep mode consumes only 25μA. A real-time clock is provided to log elapsed time, which along with a recorded temperature profile, can be used to calculate battery self-discharge.The UCC3951 monitors the individual cell voltage of three or four series-connected lithium-ion cells and provides individual cell shunt capability under microprocessor control to maintain balanced charge between cells. The UCC3951 can also drive two external high-side P-channel power MOSFETs to disconnect the cells from either the charging supply, the load, or both. For accurate cell voltage readings near full charge, a factory trimmed bandgap voltage reference in conjunction with software calibration constants stored in external memory limits overall system measurement error to 1% at 4.2V.

BLOCK DIAGRAM

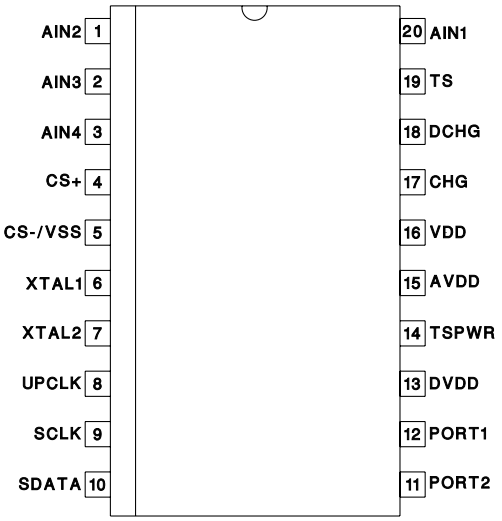


ABSOLUTE MAXIMUM RATING

VDD 20V
All other pins. . . . . VSS – 0.6V to VDD + 0.5V
Maximum Shunt Current 100mA
Maximum Power Dissipation 1000mW
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C
Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the Databook for thermal limitations and consideration of packages.

CONNECTION DIAGRAM

SOIC-20 (Top View)
DW Package



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, VDD = 14V, no load on any output, and ambient temperature T_A = 0°C to 70°C. T_A = T_J.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
Overall					
Supply Voltage	Active Mode	7.2		18	V
	Monitor Mode	6.5		18	V
Supply Current	Active Mode		5		mA
	Monitor Mode		200		µA
	Sleep Mode		20	25	µA
Clock Frequency			32.768		kHz
Serial Communication I/O (SDATA)					
High Level Input Voltage		3.5		5	V
Low Level Input Voltage				0.8	V
High Level Output Voltage				5	V
Low Level Output Sink Current	V_{OL} = 1V		1		mA
Pull Up Current			5		µA
Serial Clock Input (SCLK)					
High Level Input Voltage		3.5		5	V
Low Level Input Voltage				0.8	V
Pull Up Current			5		µA
Bidirectional Port I/O (PORT1 and PORT2)					
High Level Input Voltage		3.5		5	V
Low Level Input Voltage				0.8	V
High Level Output Voltage		2.4		5	V
Pull up Current	Pull Up Enabled		50		µA
High Level Output Source Current	V_{OH} = 4V		–1		mA
Low Level Output Sink Current	V_{OL} = 1V		1		mA
Clock Output (UPCLK)					
High Level Output Voltage		2.4		5	V
High Level Output Source Current	V_{OH} = 4V		–500		µA
Low Level Output Sink Current	V_{OL} = 1V		500		µA

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise stated, VDD = 14V, no load on any output, and ambient temperature T_A = 0°C to 70°C. T_A = T_J.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
FET Drive Output (CHG)					
High Level Output Voltage		2.4		5	V
High Level Output Sink Current	V_{OH} = 4V		–2		mA
Low Level Output Sink Current	V_{OL} = 1V		2		mA
FET Drive Output (DCHG)					
High Level Output Voltage		2.4		18	V
High Level Output Source Current	V_{OH} = 6.2V, VDD = 7.2V		–5		mA
Low Level Output Sink Current	V_{OL} = 1V		80		µA
Regulator Output (DVDD)					
Output Voltage	0 < I_{LOAD} < 15mA	4.75	5	5.25	V
Output Current				–15	mA
Thermistor Supply (TSPWR)					
Output Voltage		4.75	5	5.25	V
Output Current				–1	mA
Current Shunts (AIN1- AIN4)					
Shunt Current Capability			50	100	mA
On Resistance	V_{DS} = 2.4V, VDD = 7.2V, ID = 50mA			10	Ω
Leakage Current	Sleep Mode, V_{AINX} = 4.2V		TBD		µA
Analog to Digital Converter					
Input Voltage Range		0		5.11	V
Overall Slope (Gain) Error	Nominal Slope of 1 Bit = 5mV	–5		5	%
Gain Drift Over Temperature	T_A = 0°C to 70°C	–1		1	%FS
Offset Error	V_{ADC} = 0V	–1		1	%FS
Integral Linearity	V_{ADC} = 0.2V to 4.9V		TBD		%FS
Differential Amplifier: Current Measurement					
Current Sense Gain	CS+ = 100mV		6		V/V
Current Sense Reference Voltage	Autozero Enabled		2.5		V
Common Mode Voltage Range		–0.6		1	V
Voltage References					
Overvoltage Fault Threshold		4.18	4.25	4.32	V
Undervoltage Fault Threshold		2.2	2.3	2.4	V
Positive Current Fault Threshold	At CS+		350	400	mV
Negative Current Fault Threshold	At CS+	–400	–350		mV
Bus Timing					
Clock Frequency	See Bus Time Out			500	kHz
Clock High Time		500			ns
Clock Low Time		500			ns
SDATA and SCLK Rise Time				25	ns
SDATA and SCLK Fall Time				25	ns
Start Condition Setup Time		50			ns
Stop Condition Setup Time		50			ns
Start Condition Hold Time		50			ns
Data Input Setup Time		50			ns
Data Input Hold Time		50			ns
Data Output Hold Time				0	ns

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise stated, VDD = 14V, no load on any output, and ambient temperature T_A = 0°C to 70°C. T_A = T_J.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
Bus Timing					
Data Low Output Valid From Clock	C_{LOAD} = 50pF, I_{EXT_PU} = 300µA			200	ns
Bus Time Out		250		500	ms
Bus Free Time		50			ns
ADC Measurement					
Conversion Time	ADC is Powered Up	62.5		187.5	ms
Time From ADC Power Up to Conversion Complete		125		250	ms
Time From Conversion Complete to ADC Power Down		1		2	s
Monitor Mode					
Cycle Time (AIN1 to AIN4)	Cell Voltage Monitoring		4		ms
Current Fault Response Time	Positive/Negative Current Fault	122		244	µs
Time From Sleep Mode Disable to Monitor Mode Enable		488		976	µs

PIN DESCRIPTIONS

AIN1: This input pin serves as the current shunt connection to the positive terminal of the top cell in the series stack. The pin is also the positive terminal connection for the differential voltage measurement of the top cell. If there are only three cells in series, then this pin should be tied to AIN2.

AIN2: This input pin serves as the current shunt connection to the positive terminal of the second cell in the series stack. The pin is also the positive terminal connection for the differential voltage measurement of the second series cell, or the negative terminal connection for the differential voltage measurement of the first cell.

AIN3: This input pin serves as the current shunt connection to the positive terminal of the third cell in the series stack. The pin is also the positive terminal connection for the differential voltage measurement of the third series cell, or the negative terminal connection for the differential voltage measurement of the second cell.

AIN4: This input pin serves as the current shunt connection to the positive terminal of the fourth cell in the series stack. The pin is also the positive terminal connection for the differential voltage measurement of the fourth series cell, or the negative terminal connection for the differential voltage measurement of the third cell.

AVDD: A 10µF capacitor on this pin provides compensation and decoupling for the internal analog supply regulator.

CHG: This current-limited output pin drives an external low-side small signal bipolar transistor or MOSFET that in turn drives a high-side P-channel power MOSFET. The FET is used to disconnect the series stack of lithium-ion cells from the charging supply. The FET can be used in tandem with a second P-MOSFET, driven by DCHG, to disconnect the cells from the charging input and/or the load.

CS+: This input pin is the positive connection for a ground referenced differential current sense amplifier. The current is measured as a voltage drop across a sense resistor. The pin is also the negative terminal of the battery pack.

CS-/VSS: This pin is both the supply ground for this device as well as the negative connection for the differential current sense input. The pin should have a solid star-point ground connection to the negative terminal of the bottom cell in the stack.

DCHG: This high-voltage output pin drives an external high-side P-channel power MOSFET. The FET is used to disconnect the series stack of lithium-ion cells from the load. The pin can be used in tandem with a second FET, driven by CHG, to disconnect the cells from the charging input and/or the load.

DVDD: The output of this pin is a regulated 15mA, +5V supply from an internal linear regulator for use in powering external components, such as the system host microprocessor, as well as the internal digital circuitry. A 10µF capacitor on this pin provides compensation and decoupling for the digital supply regulator.

PORT1, PORT2: These two pins are configurable bidirectional I/O ports controlled by bits in the Port Register. They can be used to communicate with a two-wire serial EEPROM. The pins have 50µA pull ups that can be enabled or disabled when the pin is driven externally.

SCLK: This pin is an input port used to clock serial data into and out of the UCC3950. The state of SDATA is latched whenever SCLK receives a logic high data strobe

PIN DESCRIPTIONS

(clock pulse). The pin has a weak 5µA internal pull up to prevent glitches on the pin when the pack is removed from an external host.

SDATA: The SDATA pin is a bidirectional pin used for transmitting to or receiving serial data from the system host. The pin has an open source output and relies on an external pull up provided by the host. A weak 5µA internal pull up prevents glitches on the pin when the pack is removed from an external host. The serial communications protocol is described in the Serial Communications Interface section.

TS: This temperature sense pin provides an input to the ADC for battery pack temperature measurements via an external temperature sensor.

TSPWR: This output provides a switched +5V supply to external components, such as a temperature sensor or a serial EEPROM. The on/off switch is controlled by bit 7 in the Command Register, and must be active before a temperature measurement is made. Otherwise, TSPWR should be turned off to conserve battery capacity.

UPCLK: This output pin provides a 32.768kHz clock for the external host microprocessor. The clock is always present on this pin.

VDD: This pin is the power supply connection for the UCC3951. The connection to VDD must be made at the top of the series stack of cells.

XTAL1: This pin is used together with XTAL2 as the connection to the 32.768kHz crystal used for on-chip timing and the real-time clock.

XTAL2: This pin is used together with XTAL1 as the connection to the 32.768kHz crystal used for on-chip timing and the real-time clock.

APPLICATION INFORMATION

The UCC3951 has three modes of operation to provide continuous protection against current or voltage conditions outside the specifications of a lithium-ion cell while keeping power consumption to a minimum.

In the primary mode of operation, the "monitor" mode, the UCC3951 cycles through the cell voltages, constantly checking each cell for overvoltage and undervoltage faults. Charge and discharge currents are also continuously monitored to guard against short circuits across the pack terminals.

If a host requests an ADC measurement, the UCC3951 temporarily interrupts the monitoring sequence and enters an "active" mode, during which a conversion on a cell voltage is made. Once the conversion is complete, the UCC3951 reenters the monitor mode. Charge and discharge currents are still watched during the active mode, and while servicing any other command, the UCC3951 continues to monitor the cell voltages.

If both of the external FETs are opened via a host command, effectively isolating the cells from charge or discharge currents, the UCC3951 enters a power saving "sleep" mode. No monitoring of voltage or current occurs during sleep, however any command to close any one of the external FETs will restart the monitoring sequence.

MONITOR MODE

The UCC3951 always monitors the cell voltages except when the IC is

1. Making an ADC measurement (current, autozero, temperature or a cell voltage), or
2. Placed into sleep mode.

The UCC3951 continues to monitor cell voltages even if an overvoltage or undervoltage fault has already occurred, since energy may still be added or removed from the battery pack. Overcurrent conditions are always monitored, even during ADC measurements, but they are not checked when the IC is in sleep mode.

Three or Four Cells

The UCC3951 checks for overvoltage and undervoltage faults on a default number of four cells. If only three cells are used, AIN1 must be connected to AIN2 and bit 5 of Command Register 3 must be set so that an inadvertent fault condition does not occur by checking for a cell that is not present. If bit 5 is set, monitoring for overvoltage and undervoltage conditions on cell #1 is not done, although measurement of that cell is possible.

Voltage Monitoring

The UCC3951 uses a flying capacitor to monitor each individual cell for an overvoltage and an undervoltage condition. The UCC3951 cycles through each one of the four cells beginning with the cell connected to AIN1 and ending with the cell connected to AIN4. For each cell, a sequence of switches transfers the differential cell voltage to a capacitor. The cell voltage on the capacitor is then transferred to a ground referenced value and compared to both an overvoltage and an undervoltage reference.

Overvoltage Fault

An overvoltage condition exists if any individual cell voltage is greater than the overvoltage limit (4.25V/cell). As

APPLICATION INFORMATION (cont.)

a result of the fault, a bit is set in the Status Register 1 that indicates which cell is exhibiting the overvoltage condition, and CHG is driven low so that the external P-MOSFET is opened (via an external pull up and transistor), cutting off the charging current. The overvoltage fault may be cleared by discharging the battery so that the cell voltage drops into a normal operating range. The bit displaying the fault will also be cleared. Command Register 3 bit 9 will reflect the change in the CHG pin status if the external FET is opened. The host cannot overwrite this bit (that is, close the FET) until the UCC3951 senses that the overvoltage condition is removed either through the monitor mode or through a cell voltage measurement. If an overvoltage condition occurs, the external FET is opened immediately. However, the event is not latched into Status Register 1 until 30µs later. In dynamic loading situations, where a smart charger is both charging a battery and powering a load, it may be possible for an overvoltage condition to appear, cause the external FET to open, and then disappear due to the load demand before the condition is latched into the Status Register.

Undervoltage Fault

An undervoltage condition exists if any individual cell voltage is less than the undervoltage limit (2.3V/cell). As a result of the fault, a bit is set in Status Register 1 that indicates which cell is exhibiting the undervoltage condition, and the DCHG pin is driven high so that the external P-MOSFET is opened, cutting off the discharge current. The undervoltage fault may be cleared by charging the battery so that the cell voltage rises into a normal operating range. The bit displaying the fault will also be cleared. Command Register 3 bit 8 is set if the DCHG pin status if the external FET is opened. The host cannot overwrite this bit (that is, close the FET) until the UCC3951 senses that the undervoltage condition is removed either through the monitor mode or through a cell voltage measurement. Note that both an overvoltage and an undervoltage fault must never exist at the same time. If both faults do exist, the FETs connected to the CHG and DCHG pins will be forced open and sleep mode will occur. The host will be unable to override either pin, and sleep mode will prevent the UCC3951 from detecting if the condition is removed. The IC must be powered down to clear the fault.

Current Monitoring

Current flowing into or out of the battery pack is constantly monitored for excessive charge or discharge levels. The overcurrent threshold is set at ±350mV at the CS+ pin relative to the CS-/VSS pin (about ±7A based on a 0.05Ω external sense resistor) and is gained up and referenced to 2.5V to allow measurement of both charge and discharge current. The voltage across the sense resistor is measured as:

$$V_{SENSE} = (V_{CS+} - V_{CS-}) \bullet A + V_R$$

where A is the amplifier gain (x6), and V_R is an internal 2.5V reference voltage. Thus the positive current fault is set internally at 4.6V (+0.35 • 6 + 2.5V), and the negative current fault is set internally at 0.4V (–0.35 • 6 + 2.5V).

Overcurrent Fault

If an overcurrent fault exists, a bit is set in Status Register 1 indicating that a fault exists, and the CHG output is driven low and DCHG is driven high so that both of the external FETs are opened after a 122µsec to 244µsec delay. Bits 8 and 9 in Command Register 3 are set reflecting CHG and DCHG status if the external FETs are opened. The UCC3951 will also enter a low current sleep mode as a result of the opening of the FETs to conserve battery capacity.

To clear an overcurrent response, the host microprocessor must acknowledge that the fault exists by clearing bit 1 or 0 in Status Register 1 before control of bits 8 and 9 in Command Register 3 closing the external FETs are returned to the host.

SLEEP MODE

The UCC3951 enters a low power sleep if the external FETs are opened by setting bits 8 and 9 in Command Register 3. Those bits may be set by,

1. A host command, or
2. A positive or negative overcurrent fault, or
3. An overvoltage fault if the external FET on the DCHG pin is already open, or
4. An undervoltage fault if the external FET on the CHG pin is already open.

All functions except the oscillator, real-time clock, low current bandgap, and the digital supply regulator are turned off to conserve power. All commands, such as those to measure temperature, voltage, or current are still available, however some additional power up time is required. No monitoring of voltage or current occurs during sleep since the battery pack is isolated by the open external P-MOSFETs. If a host command closes either one of the FETs, the UCC3951 awakes from sleep mode and restarts the voltage and current monitoring after a brief power up time of 976µs

APPLICATION INFORMATION (cont.)

ACTIVE MODE

Writing to bits 7 - 9 in ADC Control Register 0 places the UCC3951 into active mode and kicks off an analog-to-digital conversion. Once the bits have been written to, they are locked out until the conversion is complete (that is, new ADC commands are ignored until the previous one finishes). After the conversion ends, bits 7 - 9 are cleared.

While the conversion is ongoing, the ADC Busy flag (bit 6 in ADC Control) is set. The active mode status can be observed via bit 5 of ADC Control Register 0, which is set while the ADC is powered on.

Differential Cell Voltage Measurement

A novel dual flying capacitor design is used to accurately measure the voltage across a cell for use in an algorithm controlled charge termination. This design approach allows the use of an integrating ADC while preventing measurement errors due to any charge leakage. A sequence of switch closings and openings first transfers the cell voltage to one capacitor, and then to the ADC. While the conversion begins on the first capacitor, a second capacitor is switched across the same cell and then back to the ADC. The conversion continues on the second capacitor, allowing the first capacitor to be recharged across the cell. The sequence is continued until the conversion is completed. All switches are then opened for the next measurement.

Autozero Current Sense Amplifier

For accuracy, a calibration sequence to measure offsets should be performed by the host before every current measurement. A host command to ADC Control Register 0 to autozero the current sense amplifier opens switches to CS+ and CS- and closes the amplifier inputs to ground. A conversion measures the internal 2.5V reference. This calibration value can be subtracted from a current measurement. When the conversion is complete, all switches are opened again.

Differential Current Measurement

Pack current is measured as a voltage drop across the sense resistor, and is referenced to 2.5V to allow measurement of both charge and discharge current. When the current is measured, switches connecting the current sense amplifier across the sense resistor are closed. The voltage across the sense resistor is measured as:

$$V_{SENSE} = (V_{CS+} - V_{CS-}) \bullet A + V_R$$

where A is the amplifier gain (x6), and V_R is the 2.5V reference voltage. The sense resistor voltage will be the difference between the reference and the actual reading.

Temperature Measurement

The temperature sense supply (TSPWR) is switched on only when requested by setting bit 7 in Command Register 3. A precision IC temperature sensor can be placed between this pin and ground, with its output connected to TS.

If a thermistor is used, it should be connected between TSPWR (+5V) and a fixed resistor to ground. The voltage across the fixed resistor can be measured with the ADC via TS which is ground referenced internally. The voltage on the fixed resistor will increase with temperature, and dropping most of the voltage across the fixed resistor will reduce thermistor self-heating for improved accuracy.

Thermistors come in many different types and styles, but a common type used in battery pack applications are bead type or axial-lead thermistors with a typical value of 10kΩ at 25°C. Using a voltage divider consisting of a 10kΩ fixed resistor and a 10kΩ at 25°C thermistor in a configuration shown in Figures 3 and 4, a relatively linear change in voltage with temperature is developed at TS.

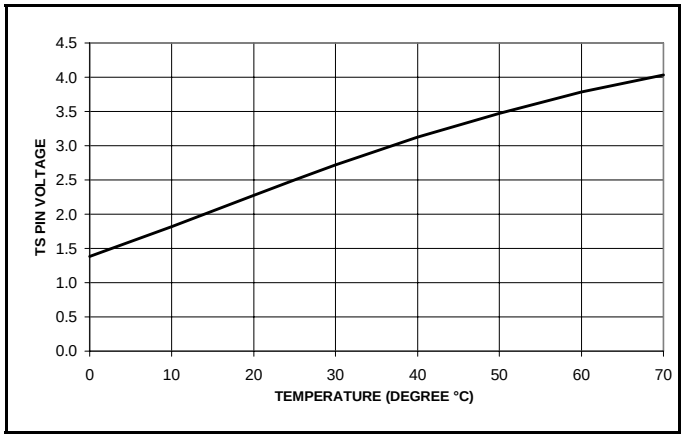


Figure 1. Thermistor Voltage vs Temperature

Analog To Digital Converter (ADC)

The ADC is used for measurement of the individual cell voltages, battery pack temperature and pack current. An ADC measurement is made whenever a combination of bits 7 - 9 in ADC Control Register 0 are set. The ADC has 10 bit resolution, and the design is based on a delta-sigma modulator. A pulse density modulated one-bit stream representing the measured voltage is integrated in a counter that can be read via ADC Conversion Register 4. The conversion complete status can be polled by the host via bit 6 in ADC Control Register 0.

APPLICATION INFORMATION (cont.)

To conserve energy, the ADC powers itself on whenever an ADC measurement is requested, and it powers itself down within 1 to 2 seconds after the last conversion (unless, of course, a measurement is requested within that time). The power up status can be checked with bit 5 in ADC Control Register 0.

If the real-time clock is stopped (via bit 8 in Register 5) while the ADC is powered on, then the ADC will remain powered on. When the timer is released, the ADC will power down 1 to 2 seconds later.

Voltage References

The UCC3951 contains a temperature stable on-chip bandgap voltage reference that is used by the ADC, voltage and current monitoring references, and the linear voltage regulators. Due to the accuracy requirements for the voltage readings of lithium-ion cells, the bandgap is trimmed to better than ±1%. The voltage monitoring references are derived from the bandgap, and are set at 4.25V for the overvoltage fault and 2.3V for the undervoltage fault. The current monitoring references are set at 4.6V for the positive current fault and 0.4V for the negative current fault.

Linear Voltage Regulators

Two voltage regulators provide the supplies to the internal analog and digital circuitry, as well as the external host microprocessor, EEPROM, and thermistor. Compensation and decoupling of both these supplies is required at AVDD and DVDD with 10µF capacitors. The nominal output voltage on both DVDD and TSPWR is approximately 5V.

Current Shunts

Four current shunts are available to direct 50mA nominal around each cell to provide for charge equalization. Each switch has a maximum resistance of 10Ω at 50mA. Power must be dissipated in external resistors connected to the positive and negative terminals of each cell. If shunts are not required in the application, the resistors shown in Figures 3 and 4 are not necessary.

Control of each shunt is done via bits 1 - 4 in Command Register 3. If a shunt is closed, overvoltage and undervoltage monitoring of that cell is ignored, although a measurement of the cell is possible. If an overvoltage or undervoltage fault occurs on a cell and that cell is then shunted, the fault condition will not be cleared since the cell is not monitored.

Only one cell should be shunted at any one time, although shunting more than one is allowed. While charging the battery, the cell with the highest voltage as measured with the ADC should be shunted first. Conversely, on discharge, the cell with the lowest voltage should be shunted first.

External MOSFET Drivers

The CHG and DCHG pins drive external P-MOSFETs that are used to isolate the series stack of cells from the charging supply and load. The P-MOSFET connected to the charging supply must be driven with a low side small signal bipolar or MOSFET (the CHG output is a current limited output.) The P-MOSFET with its gate pulled up by the stack of cells is driven directly by the DCHG pin.

Crystal Oscillator

A low current 32.768kHz crystal oscillator provides the clock to the internal logic, as well as to the host microprocessor. The clock is active even during sleep mode so that the UCC3951 can respond to host commands.

Real-Time Clock

A 26-bit real-time clock is available to log parameters such as storage time. The clock is updated every second. Twenty-six bits provides more than two years of elapsed time measurement for extended battery pack storage periods. The real-time clock can be cleared via bit 0 in the Command Register. If more than two years elapse, bit 7 in the Real-Time Clock Register 5 is set, and the real-time clock overflows. The real-time clock is broken up into three 10-bit registers. Reading all three registers requires a separate Read Data command for each register. To prevent the clock from updating while the registers are read, the following sequence should be used:

1. Set the Stop Timer bit 8 in the Real-Time Clock Register 5. This action halts the clock, and stores up to one second of elapsed time during which the real-time clock can be read.
2. Read all three real-time clock registers in one second.
3. Clear the Stop Timer bit to restart the real-time clock and to update the clock by the stored elapsed time.

Note that if the Stop Timer bit is not cleared, the timer stays halted. Also note that if it takes the host longer than one second to complete the sequence, the real-time clock will be inaccurate.

Bidirectional I/O Ports

Two pins (PORT1, PORT2) are provided for use as bidi-

APPLICATION INFORMATION (cont.)

rectional ports under host control. Six bits in Port Register 2 provide control over the direction of data flow, the value of the bit to be sent, and whether a pull up should be engaged to pull the pin high when data is not being sent. All input or output data uses +5V to equal a logic high.

When reading the ports configured as inputs, the value returned to the host represents the state of the pin, not the values in the Port Register 2. When reading the ports configured as outputs, the value returned to the host is the same as the value in the Port Register 2.

If these ports are used as an EEPROM interface, a standard two wire bidirectional interface can be implemented using one port as clock and the second port as data. Open collector outputs are typically used on EEPROMs, so the pull ups on the ports may be engaged.

Serial Communications Interface

The UCC3951 supports a bidirectional two wire bus and serial data transmission protocol for communicating with a host microprocessor. The bus is controlled by the host. Since the clock speed of the host microprocessor may be unknown, a clock pulse on SCLK must accompany each data bit on SDATA. The SCLK clock may operate asynchronous from the UCC3951 clock. All input clock and data or output data uses +5V to equal a logic high.

The data protocol is defined as follows (see also Figure 4).

BIT	DRIVEN BY	DATA CONTENT
X	Host	Start Configuration
0	Host	Read/Write (R/W) Direction Bit 1 for READ, 0 for WRITE
1	Host	Register Address Bit 2 (MSB)
2	Host	Register Address Bit 1
3	Host	Register Address Bit 0 (LSB)
4	WRITE: Host READ: UCC3951	Data Bit 9 (MSB) from Addressed Register
5 - 12	WRITE: Host READ: UCC3951	Data Bit 8 to 1 from Addressed Register
13	WRITE: Host READ: UCC3951	Data Bit 0 (LSB) from Addressed Register
X	Host	Stop Condition

Two commands are available to move data to or from the UCC3951. They are:

1. Read Data (from the UCC3951)
2. Write Data (to the UCC3951)

The host determines which command is activated via a Read/Write (R/W) direction bit included in every data transmission. Read Data or Write Data commands are always 14 bits long, even if the register contains less than 10 bits of data. Any unused or reserved bits should be written with a zero to account for future upgrades. Valid data is indeterminate on unused bits.

Data on SDATA must remain stable whenever SCLK is high. Changes in the data during a high SCLK will be interpreted as a Start or Stop condition. A Start condition must precede a data transmission, and a Stop condition must follow.

Write Data: On a Write Data command, the Stop condition writes the data into the addressed register. The R/W and Address bits are clocked in on the rising edge of SCLK, but the remaining Data bits are clocked in on the falling edge of SCLK.

The Write Data command can be interrupted with an early Stop condition at any time during data transfer. However, if more than 14 bits are inadvertently clocked in (a late Stop condition), the command is canceled. The command is also canceled if a second Start condition is received before a Stop condition.

Read Data: After the R/W and three Address bits of a Read Data command are clocked in, the UCC3951 takes control of the bus to send data to the host. The R/W and Address bits are clocked in on the rising edge of SCLK, but the remaining Data bits are clocked out on the falling edge. The Read Data command can only be canceled before the UCC3951 controls the bus. Once control is taken by the UCC3951, early Stop conditions or repeated Start conditions are ignored. The data of the addressed register must be clocked out via SCLK before the UCC3951 releases control of the bus and a new command can be accepted. If more than 14 bits are clocked out without a Stop command, the extra bits are indeterminate.

If a command is not completed within 250ms, the bus times out and the previous command is terminated. A new Start condition is required before the next command.

APPLICATION INFORMATION (cont.)

Registers

Eight 10-bit wide registers are available for monitoring and controlling the operation of the UCC3951. The ADC Control Register 0 controls ADC measurements and provides the status of the analog to digital converter. The Status Register 1 indicates if any fault conditions have occurred. The Port Control Register 2 writes and reads data on the PORT1 and PORT2 pins. The Command Register 3 provides the control and status of the shunts and the CHG, DCHG and TSPWR pins. The ADC Conversion Result Register 4 is the output of the ADC. The register is overwritten upon the completion of a conversion. The three Real-Time Clock Registers contain the data and control for the real-time clock.

Register Map

ADDRESS	REGISTER
0	ADC Control Register
1	Status Register
2	Port Control Register
3	Command Register
4	ADC Conversion Register
5	Real Time Clock (MSB) and Control Register
6	Real Time Clock Register
7	Real Time Clock (LSB) Register

Register 0: ADC CONTROL

Bit 9	Bit 8	Bit 7	Read/ Write	FUNCTION
0	0	0	R/W	All Channels Open
0	0	1	R/W	Measure Cell #1 Voltage
0	1	0	R/W	Measure Cell #2 Voltage
0	1	1	R/W	Measure Cell #3 Voltage
1	0	0	R/W	Measure Cell #4 Voltage
1	0	1	R/W	Measure Temperature
1	1	0	R/W	Measure Current
1	1	1	R/W	Autozero Current Sense Amplifier
BIT 6			R	ADC Busy (1) / ADC Ready (0)
BIT 5			R	ADC Power On (1) / Off (0)
BIT 4			-	-
BIT 3			-	-
BIT 2			-	-
BIT 1			-	-
BIT 0			-	-

Register 1: STATUS

Bit	Read/ Write	Function
9	R	Overvoltage on Cell #1 (1); Condition Cleared (0)
8	R	Overvoltage on Cell #2 (1); Condition Cleared (0)
7	R	Overvoltage on Cell #3 (1); Condition Cleared (0)
6	R	Overvoltage on Cell #4 (1); Condition Cleared (0)
5	R	Undervoltage on Cell #1 (1); Condition Cleared (0)
4	R	Undervoltage on Cell #2 (1); Condition Cleared (0)
3	R	Undervoltage on Cell #3 (1); Condition Cleared (0)
2	R	Undervoltage on Cell #4 (1); Condition Cleared (0)
1	R/W	Positive Current Fault (1); Condition Cleared (0)
0	R/W	Negative Current Fault (1); Condition Cleared (0)

Register 2: PORT CONTROL

Bit	Read/ Write	Function
9	R/W	Write Out Port #1 (1); Read In Port #1 (0)
8	R/W	Set Port #1 (1); Clear Port #1 (0)
7	R/W	Enable Port #1 pull up (1); Disable Port #1 pull up (0)
6	R/W	Write Out Port #2 (1); Read In Port #2 (0)
5	R/W	Set Port #2 (1); Clear Port #2 (0)
4	R/W	Enable Port #2 pull up (1); Disable Port #2 pull up (0)
3	-	reserved
2	-	reserved
1	-	reserved
0	-	reserved

Register 3: COMMAND

Bit	Read/ Write	Function
9	R/W	CHG Output High (1); CHG Output Low (0)
8	R/W	DCHG Output Low (1); DCHG Output High (0)
7	R/W	TSPWR Output On (1); TSPWR Output Off(0)
6	R/W	Real-Time Clock Reset (1)
5	R/W	Three lithium-ion Cells (1); Four lithium-ion Cells (0)
4	R/W	Shunt Cell #1 Closed (1); Shunt Cell #1 Open (0)
3	R/W	Shunt Cell #2 Closed (1); Shunt Cell #2 Open (0)
2	R/W	Shunt Cell #3 Closed (1); Shunt Cell #3 Open (0)
1	R/W	Shunt Cell #4 Closed (1); Shunt Cell #4 Open (0)
0	-	-

APPLICATION INFORMATION (cont.)

Register 4: ADC CONVERSION RESULT

Bit	Read/ Write	Function
9	R	ADC Conversion MSB
⇓	⇓	™
0	R	ADC Conversion LSB

Register 5: REAL-TIME CLOCK (MSB)

Bit	Read/ Write	Function
9	-	Reserved
8	R/W	Stop Timer (1), Start Timer (0)
7	R/W	Overflow of Real-Time Clock (1); Clear Overflow (0)
6	-	-
5	R	Real-Time Clock MSB (Bit 26)
⇓	™	⇓
0	R	Real-Time Clock (Bit 20)

Register 6: REAL-TIME CLOCK

Bit	Read/ Write	Function
9	R	Real-Time Clock (Bit 19)
⇓	™	⇓
0	R	Real-Time Clock (Bit 10)

Register 7: REAL-TIME CLOCK (LSB)

Bit	Read/ Write	Function
9	R	Real-Time Clock (Bit 9)
⇓	™	⇓
0	R	Real-Time Clock LSB (Bit 0)

Figure 3 shows the UCC3951 in a typical three cell battery pack application, incorporating a serial EEPROM to store battery data. The pack communicates with an external processor via the serial data and clock lines. The EEPROM is powered from the switchable TSPWR output to minimize current draw when not being used.

Low RDS_{ON} P-channel MOSFET's Q1 and Q2 control the charge and discharge currents respectively. High side switching is used to prevent opening of the ground line, and buffers the UCC3951 from the open-circuit voltage of the battery charger. The ground reference for the UCC3951 is referenced to the top of the current sense resistor to prevent CS+ from going several volts below substrate during a high current discharge pulse. The normal voltage drop between this ground reference and Pack (-) is only a few hundred millivolts maximum.

The gate of Q1 requires level shifting, performed by Q3, to stand off the open circuit charger voltage in the case of a charger fault. This can be done with a small N-channel MOSFET as shown, or with a bipolar transistor such as a 2N2222. The source current of the totem pole CHG output is internally limited to a few milliamps, so no base resistor is required if a bipolar is used. Note that this will increase the current draw whenever Q1 is turned on. Although the body diode will allow discharging with Q1 off, it would normally be turned on during discharge to minimize losses.

The gate of Q2 is driven directly by a totem pole style output, so no gate to source resistor is required. Note, however, that the sink current is internally limited by a 14K resistor. This was done to facilitate slew rate limiting. Adding a series RC from drain to gate will slew rate limit the output voltage of Q2, minimizing surge currents into highly capacitive loads (which may otherwise cause a current fault). An example is shown in Figure 2. Another alternative is to have the host retry several times by turning Q2 back on after a delay. This hiccup mode of operation will only work if the load capacitor is not discharged during the off time. The on-off duty cycle must be chosen so as not to exceed the safe operating area of Q2 under the applied conditions.

The nominal current fault delay of 183µsec is intended to allow charging of some capacitive loads while maintaining effective short circuit protection. A longer delay could destroy Q1 and Q2 under short circuit conditions due to the high short circuit current of some battery packs. The problem is compounded by the drop in battery voltage due to internal resistance. This drop reduces gate bias and may cause Q2 to operate in the linear region, raising power dissipation even further. (The power dissipation of Q1 is lower because its body diode becomes forward biased.)

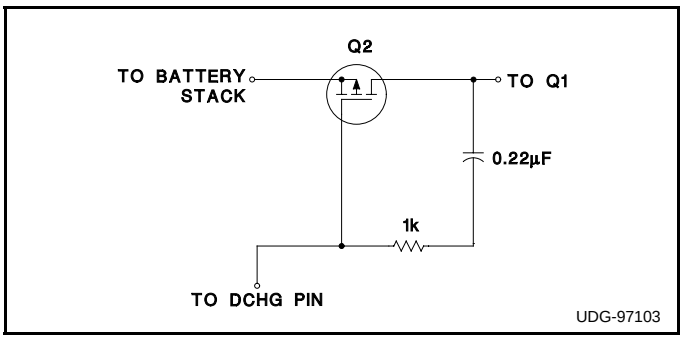


Figure 2. Slew Rate Limiting Discharge FET Turn On to Reduce Surge Current into Capacitive Loads

APPLICATION INFORMATION (cont.)

The circuit in Figure 4 shows a four cell pack with an internal host microprocessor. It may be powered from the regulated DVDD output. A clock is provided for the micro on pin 8. Also shown are two components to protect the gate of Q1 from possible overvoltage in cases where the charger open circuit voltage may exceed 20V.

To prevent the voltage on VDD from dropping below the UCC3951's minimum operating threshold during a short, an RCD may need to be added to hold up the VDD supply for a maximum of 244µsec. This is shown in Figure 4. The resistor value should be small enough to keep the drop across it less than 350 mV at full VDD load current. This includes whatever load current is applied to DVDD and TSPWR. Values of the resistor and capacitor, for three and four cell packs, are shown in Figure 4 The schottky diode prevents VDD from falling more than a diode drop below AIN1 when the battery voltage suddenly rises.

If cell balancing is required, the shunt current for each cell must be limited to less than 100 ma by an external resistor (R2, R3 and R6 in Figure 4). Note that a resistor is not required in series with the positive input of the top cell or the negative input of the bottom cell. (Only one cell should be shunted at a time.) To prevent shorting out the cell stack, never turn on all current shunts at once.

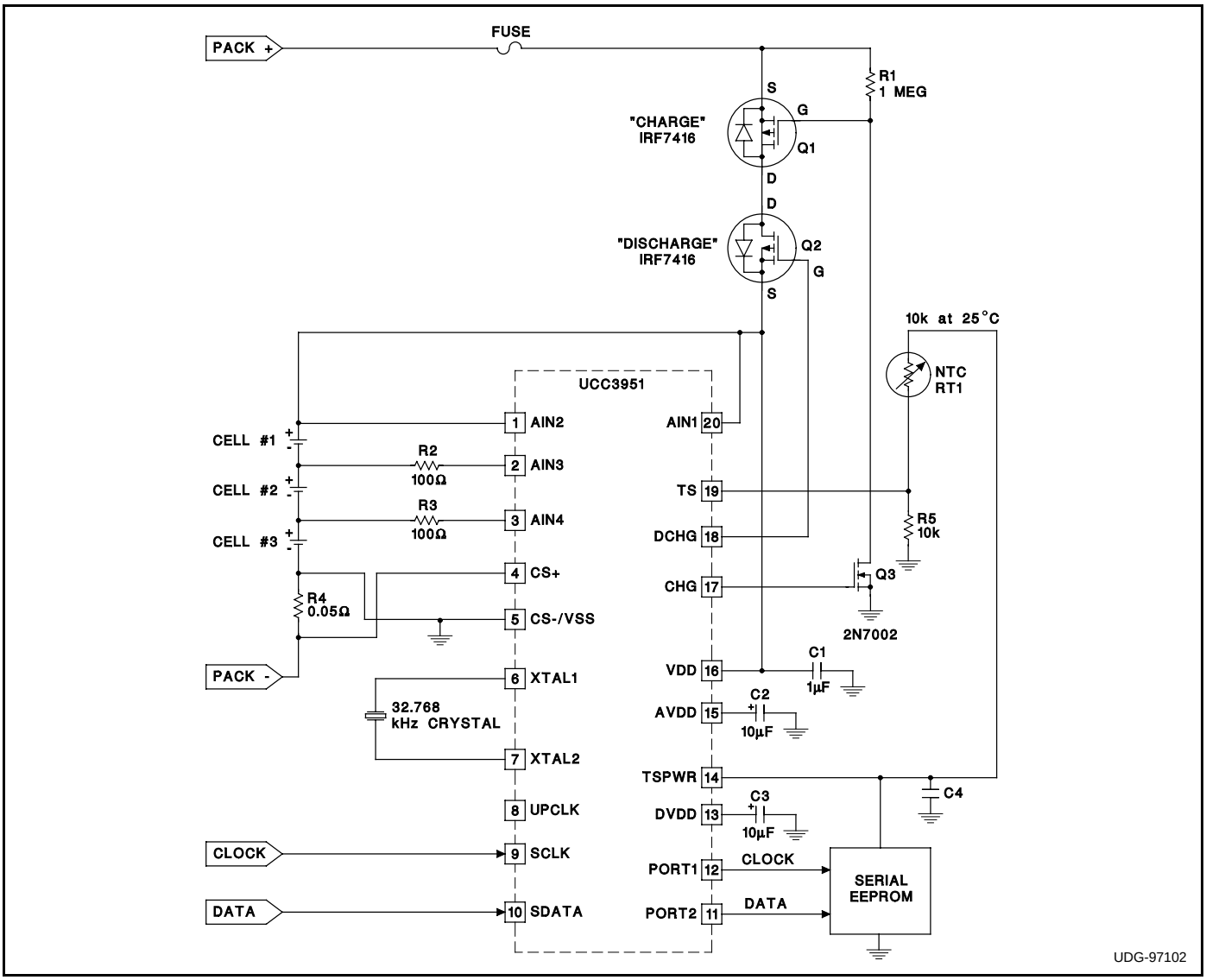


Figure 3. Three Cell Pack with EEPROM

APPLICATION INFORMATION (cont.)

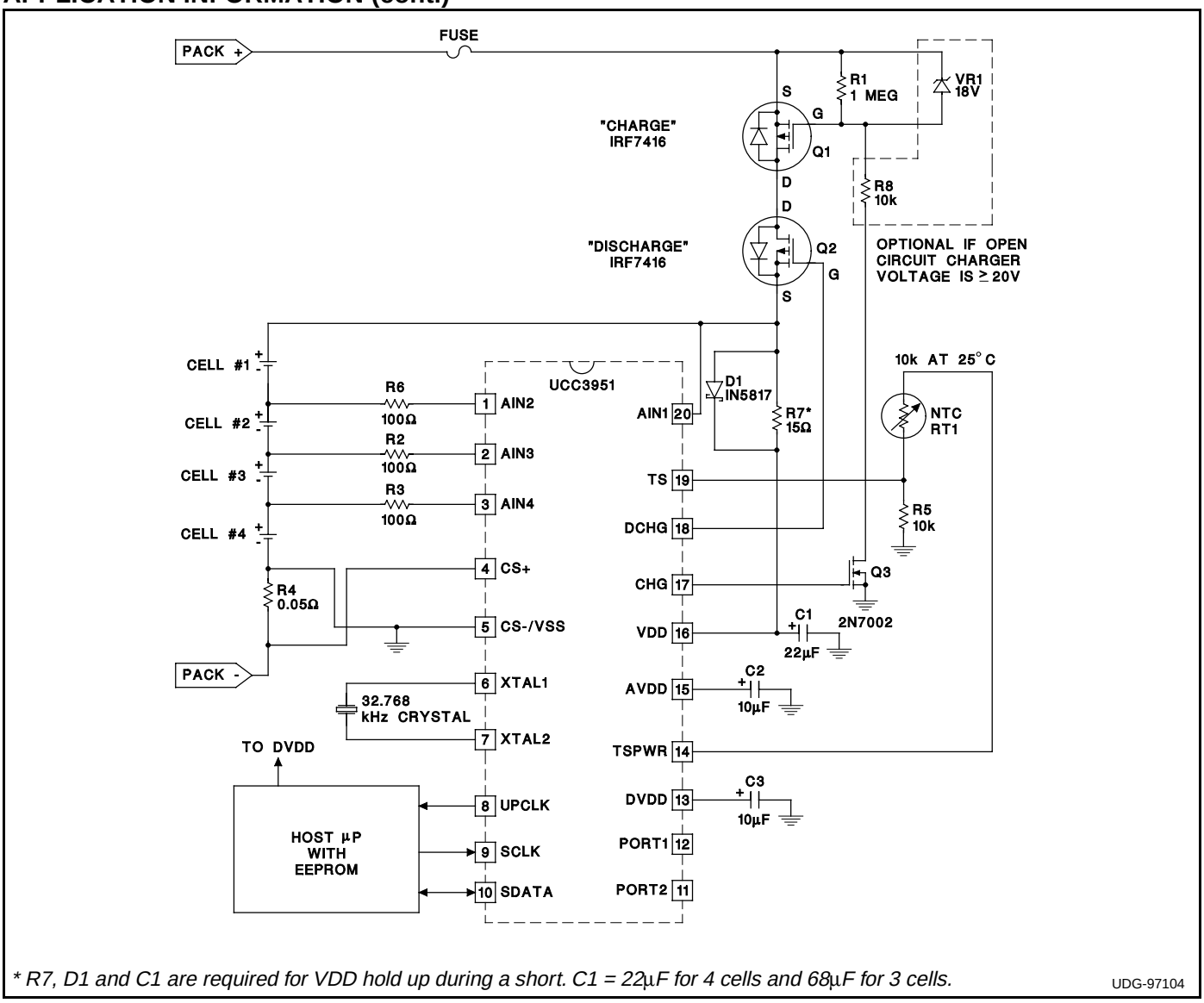


Figure 4. Four Cell Pack withHost Microprocessor

System Calibration Strategy

Calibrating the voltage measurement channels connected to each of the four cells is necessary to meet the 1% tolerance on voltage measurement at 4.2V that is required for proper charge termination of lithium-ion cells. At the factory, the bandgap reference is trimmed to better than 1% tolerance to provide an accurate internal reference over temperature. The ADC is capable of 0.1% resolution (10 bits) at 4.2V. At final system test, a simple software calibration of each of the voltage measurement channels should be performed to obtain the highest accuracy. The test requires an accurate external voltage reference (to 1%) near 4.2V placed between one pair of AIN pins. A conversion on that external reference will provide a digital number representing the reference voltage. The number should be stored in external memory (host memory or EEPROM), and can be used in the following equation to calibrate future readings on that channel:

$$\text{Actual Voltage} = \text{ADC Reading} \bullet \frac{\text{Reference Voltage}}{\text{Reference ADC Reading}}$$

Channel calibration can also be done at different temperatures together with a thermistor reading to provide an accurate calibration of the channel as ambient temperature changes.

APPLICATION INFORMATION (cont.)

Calibration of the current measurement channel is done by setting the autozero bit 6 in Command Register 3. The inputs to the current sense differential amplifier are closed to ground, and an conversion is made. The autozero bit is cleared, switches are opened, and a digital number representing zero current can be read and stored in external memory.

TIMING DIAGRAMS (SERIAL INTERFACE)

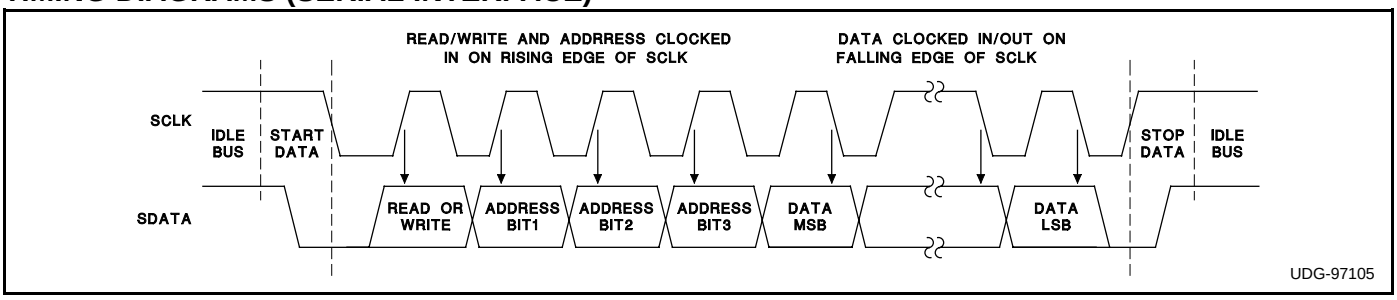


Figure 5: Serial Bus Protocol

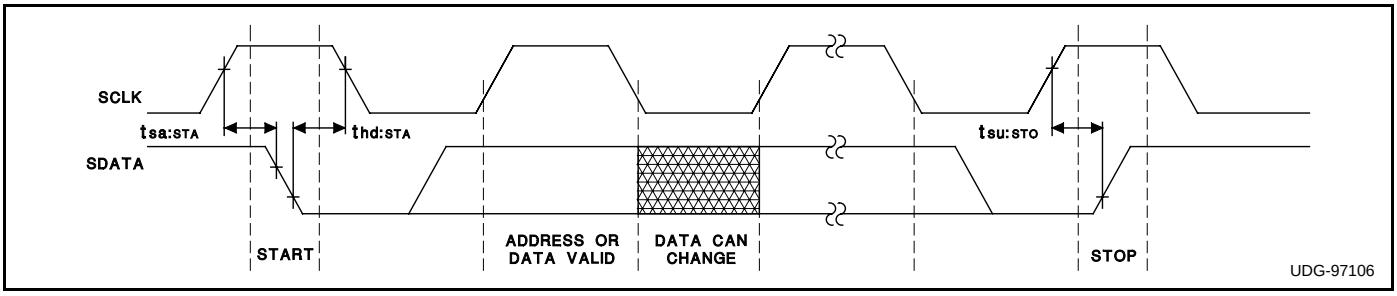


Figure 6: Serial Bus Start and Stop Condition Timing

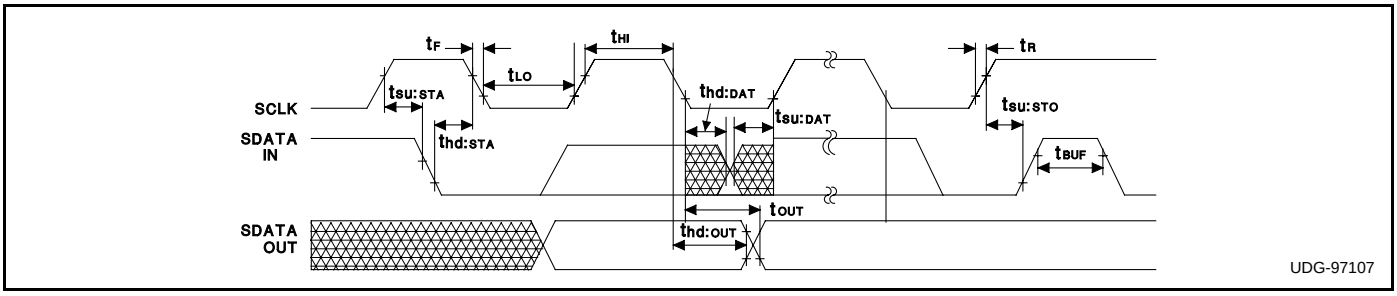


Figure 7. Serial Bus Timing Information

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